March 30, 2004

Errata Document for CY7C637xx / enCoRe™ USB Combination Low-speed USB & PS/2 Peripheral Controller

This document describes the errata for the enCoRe™ USB Combination Low-speed USB & PS/2 Periheral Controller / CY7C637xx. Details include errata trigger conditions, available workarounds, and silicon revision applicability. This document should be used to compare to the datasheet for this device to fully describe the device functionality.

Please contact your local Cypress Sales Representative if you have further questions.

Part Numbers Affected

Part Number	Device Characteristics
CY7C63722	All packages
CY7C63723	All packages
CY7C63743	All packages

enCoRe™ USB Combination Low-speed USB & PS/2 Peripheral Controller Qualification Status

Product status: In Production - Qual report: 001406

enCoRe™ USB Combination Low-speed USB & PS/2 Peripheral Controller Errata Summary

The following table defines the errata applicability to available enCoRe™ USB Combination Low-speed USB & PS/2 Peripheral Controller family devices. An "X" indicates that the errata pertains to the selected device.

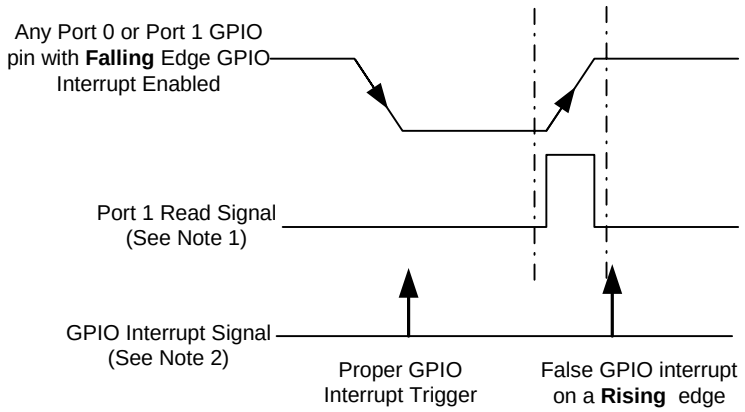
Note: Errata titles are hyperlinked. Click on table entry to jump to description.

Items	CY7C637xx	Rev Letter	Fix Status
1. Faulty GPIO Interrupt	X	A	No silicon fix planned.

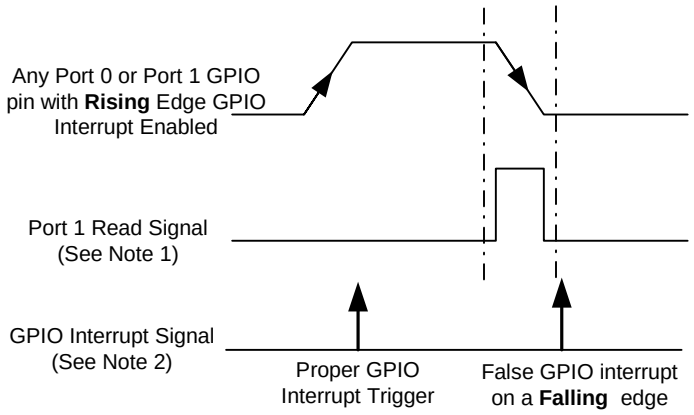
1. Faulty GPIO Interrupt

- **PROBLEM DEFINITION**

  When a falling edge interrupt is enabled for a GPIO pin, reading the GPIO Port 1 coincident to a rising edge of that GPIO signal may generate a false GPIO interrupt.



When a rising edge interrupt is enabled for a GPIO pin, reading the GPIO Port 1 coincident to a falling edge of that GPIO signal may generated a false GPIO intterupt



Note 1: Port 1 Read is an internal signal that is asserted when Port 1 is read with an "IORD 01h" instruction.

Note 2: The GPIO Interrupt signal is an internal signal. The arrow indicates that a GPIO interrupt is triggered.

- **PARAMETERS AFFECTED**

  Interrupts

- **TRIGGER CONDITION(S)**

  Reading the GPIO Port 1 when either rising or falling edge interrupts are enabled for a GPIO pin.

- **SCOPE OF IMPACT**

  The chip enters the GPIO Interrupt Service Routine (ISR) in error.

- **WORKAROUND**

  Workarounds will need to be tailored to individual applications based on the flexibility of changing the GPIO usage, the timing of the GPIO interrupt sources and firmware interrupt latencies.

- **FIX STATUS**

  No silicon fix is planned.

References

1. 38-08022 CY7C63722/23/43 enCoRe™ USB Combination Low-speed USB & PS/2 Peripheral Controller datasheet.

Document History Page

Document Title: CY7C637xx Rev. A Errata Document Number: 38-17015				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0		March 14, 2003	bon	Initial release
1.1		May 1, 2003	bon	Added pictures to clarify the issus.
**	215104	See ECN	bha	Enter errata into spec system